High-Performance GaAs Heterojunction Bipolar Transistor Monolithic Logarithmic IF Amplifiers

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Abstract—**The GaAs/AlGaAs heterojunction bipolar transistor (HBT) technology is used to demonstrate high-performance monolithic logarithmic intermediate frequency (IF) amplifiers. These log IF amplifiers, believed to be the first using the HBT technology, implement both "true" and "successive-detection" designs. Monolithically cascaded log gain stages are used to achieve piecewise-approximated logarithmic functions for the compression of wide-dynamic-range signals. An HBT IC fabrication process, based on a 3 μm emitter, self-aligned base ohmic metal transistor employing both molecular-beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) growth structures, is used to advance the state of the art in monolithic log IF amplifier technology. The true log amp integrates four dual-gain (limiting and unity gain) stages without on-chip video detection. Its performance includes dc–3 GHz IF/video bandwidth, 400 ps rise time, $< \pm 1$ dB log error over ≈ 40 dB dynamic range at 3 GHz, and a tangential signal sensitivity (noise) of -60 dBm (test set limited). The successive-detection log amp, designed for lower frequency and dynamic range, employs three limiting gain stages and four detector stages to achieve a 550 MHz bandwidth and $< \pm 0.34$ dB log error over a 27 dB dynamic range. It is able to process 13 ns pulses with 5.0 ns and 5.2 ns rise and fall times, respectively.**

I. INTRODUCTION

LOGARITHMIC amplifiers are critical components in radar, electronic warfare (EW), sonar/ultrasound, and instrumentation applications requiring the compression of wide-dynamic-range signals, beyond the usefulness of linear amplification (e.g. automatic gain control). Typical applications include phased-array antennas, monopulse direction finding, target identification, electronic countermeasures (ECM), sonar signal amplification, ultrasound scanning, and power measurement.

Logarithmic amplifiers are classified [1] into two general types: 1) detector-log video amplifiers (DLVA's) and 2) log intermediate frequency (IF) amplifiers. In DLVA's the modulated RF input signal (up to 26 GHz) is first detected using tunnel or Schottky diodes, and the resulting low-frequency video signal (10–100 MHz range) is logarithmically amplified. In log IF amplifiers the RF input is first down-converted to IF (1–3 GHz range), logarithmically amplified, and detected. While the DLVA offers higher input frequency performance by virtue of the front-end detector, frequency information is lost through the initial video detection. The log IF amp maintains frequency information, but requires down-converted signals and higher frequency logarithmic amplification capability than the DLVA, which requires only low-frequency video logging. The latter enables the log IF amp to have generally superior pulse characteristics and greater instantaneous input dynamic range, up to 80 dB for hybrid-cascaded versions. However, the key limitations of present-day logarithmic amplifiers in achieving the higher performance levels are high complexity (cost), high power consumption, and large size.

Bipolar transistors offer attractive advantages over field-effect transistors in differential amplifier performance critical for log amp applications. These include exponential-based nonlinear function, better device matching, higher transconductance and output impedance for higher gain and lower distortion, and lower trapping effects and $1/f$ noise. The first GaAs MESFET true log IF amplifier reported [2] uses six hybrid-cascaded log stages to achieve a 70 dB dynamic range from 0.5 to 4 GHz, but has relatively high log error (± 3.5 dB) and power consumption (≈ 5 W). Silicon bipolar hybrid log amps have demonstrated similar dynamic range with smaller error and lower power consumption, although the operational frequencies are limited to ≈ 1–2 GHz [1], [3]. The GaAs heterojunction bipolar transistor (HBT) offers improved speed, power, and gain performance over both silicon bipolar and GaAs MESFET with significantly relaxed fabrication requirements. Relaxed emitter lithographic dimensions of ≈ 3 μm are adequate to achieve HBT transistors with f_t and f_{max} in the range of 20–40 GHz. The availability of semi-insulating GaAs substrate for circuit integration is also attractive for reduced parasitic capacitance as well as simplifying device isolation. The HBT technology has already demonstrated state-of-the-art analog-to-digital conversion circuits [4], [5] and microwave/millimeter-wave devices [6], [7]. This paper describes initial monolithic logarithmic IF amplifier results obtained with an HBT IC fabrication process designed for RF analog applications. The HBT technology appears attractive for realizing higher performance log amps with reduced complexity, power, and size.

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II. Log IF Amplifier Design

Logarithmic IF conversion can be implemented as a "true" (Fig. 1) or a "successive-detection" log IF (Fig. 2) amplifier when using the piecewise-approximation technique with cascaded stages [1]. In this work both log IF amplifier types were investigated using the GaAs HBT technology. Each stage of the cascaded log amp uses a limiting amplifier achieved with an emitter-coupled differential HBT pair. As the input signal level increases, more amplifier stages limit, and a piecewise approximation to the log function is achieved. The total dynamic range and accuracy are determined by the number of stages and the gain of each stage. The higher the gain, the greater the inaccuracy; the gain of each stage then determines the number of stages needed to achieve the dynamic range. The ultimate monolithic dynamic range and accuracy are limited by the bandwidth, noise or tangential signal sensitivity (TSS), and chip feedback characteristics (isolation), which can cause oscillation problems. Differential circuit techniques can be used to reject common-mode spurious signals from the bias or ground lines and eliminate oscillation resulting from multistage gain feedback through the common substrate.

In the true log IF amp, video detection is performed after the cascaded log functions, while in the successive-detection approach, detection is performed after each logging stage and the outputs are summed. The true log IF amp is termed true because the carrier output is proportional to the log of the carrier input, and phase information is inherently preserved by the serial logging stages. In the successive-detection approach the carrier output is the limited carrier input, and phase information is not preserved due to phase delays associated with the successive detection and summation. However, it can be compensated for with delay lines or made negligible by using very wide band stages. Compared to the true log IF, the successive-detection approach places a less stringent dynamic range requirement on the detector; the true log IF requires video detection over the total logged dynamic range while successive detection requires only a single logged stage detection.

A. HBT True Log IF Amplifier

The GaAs HBT true log IF amplifier, shown schematically in Fig. 3, is implemented as a monolithic, fully differential four-stage design without on-chip video detection. The number of monolithically cascaded stages was conservatively limited for the initial design. The component log stage is based on a Si bipolar dual-gain stage design consisting of parallel-combined limiting and unity gain amplifiers [8]. The dual-gain log stage is realized with the emitter-coupled differential HBT amplifier combination shown in Fig. 4; each is dc coupled to the adjacent stage. For the HBT log IF amp, the gain of the log stage was designed to be 12 dB, yielding a total four-stage dynamic range of 48 dB. While the use of differential circuit techniques minimizes the effects of noise and isolation feedback in the monolithic integration, the incorporation of additional log stages is limited ultimately by the noise performance. To achieve a wider dynamic range log amp, two monolithic four-stage log amps can be hybrid cascaded with filtering to achieve ≈ 80 dB dynamic range. The HBT log amplifiers have an intrinsic operational frequency range from dc to ≈ 3 GHz; however the actual useful bandwidth is governed by the signal sensitivity or noise requirements.

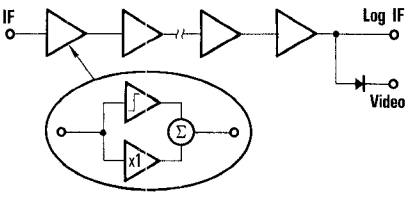


Fig. 1. Schematic diagram of "true" logarithmic IF amplifier with cascaded dual-gain (limiting and unity gain) log stages; carrier output is proportional to the log of the carrier input.

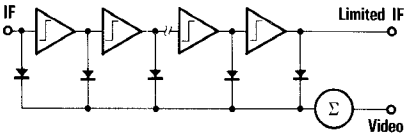


Fig. 2. Schematic diagram of "successive-detection" logarithmic IF amplifier with cascaded limiting gain log stages and summed detector outputs; carrier output is the limited carrier input.

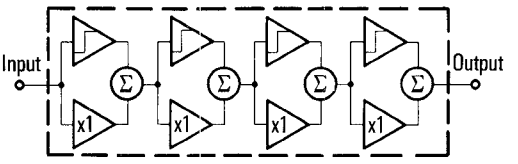


Fig. 3. Block diagram of the HBT monolithic four-stage true log IF amplifier with cascaded dual-gain log stages and without on-chip detection; the log amp is fully differential.

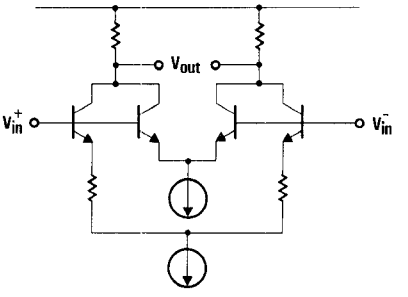


Fig. 4. Circuit schematic of dual-gain log stage, implemented with emitter-coupled differential amplifiers, used in the HBT monolithic four-stage true log amp.

B. HBT Successive-Detection Log IF Amplifier

The GaAs HBT successive-detection log IF amplifier, shown schematically in Fig. 5, is implemented as a monolithic, fully differential four-stage design with three limiting gain stages and four detector stages. As in the true log amp design, the number of monolithically cascaded stages was conservatively limited for the initial evaluation. The component log stage uses an emitter-coupled differential amplifier for the limiter and a balanced

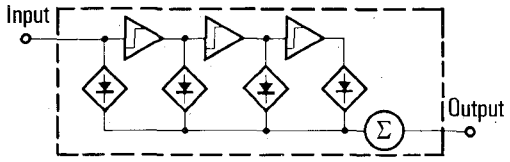


Fig. 5. Block diagram of the HBT monolithic four-stage successive-detection log IF amplifier with three limiting gain stages and four detectors; the log amp is fully differential.

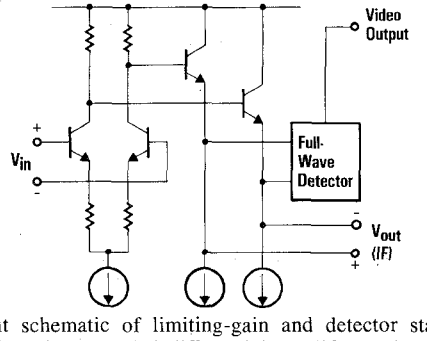


Fig. 6. Circuit schematic of limiting-gain and detector stages, implemented with emitter-coupled differential amplifier and transistor full-wave rectifier, used in the HBT monolithic four-stage successive-detection log amp.

full-wave HBT rectifier for the detector, as shown in Fig. 6. The log stages are dc coupled on both the RF and the video signal path. The video signals from the detectors are summed into a resistor, with the summing point used as the video output since the circuit has no video amplifier. Due to the wide bandwidth of the limiting gain stages, no delay lines are required in the summation of the video signal lines. An optional on-chip video filter is available; however, for application-specific video bandwidths, an off-chip filter can be used. While the overall successive-detection log IF circuit is fully differential, including the limiting amplifiers and the detectors, the input and IF outputs can be either single-ended or differential; the video output is single-ended.

III. HBT Log Amp IC Fabrication Technology

The monolithic log IF amplifiers were fabricated with a 3 μm emitter, self-aligned base ohmic metal (SABM) HBT IC fabrication process designed for baseband/RF analog applications. The self-aligned HBT process is an enhanced version of the baseline non-self-aligned HBT IC process, which has already demonstrated state-of-the-art analog/digital (A/D) conversion circuits [4], [5]. This same process is also being used for advanced LSI A/D and microwave device/IC applications. Both molecular-beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) growth techniques were used for the HBT log amp fabrication.

MBE HBT epitaxy offers an attractive combination of technology maturity and excellent growth parameter control for high performance while MOCVD offers potential advantages of higher throughput and lower cost with nearly comparable performance. The GaAs/AlGaAs n-p-n HBT emitter-up, single heterostructure shown in Fig. 7 was used for both MBE and MOCVD log amp epitaxy. It

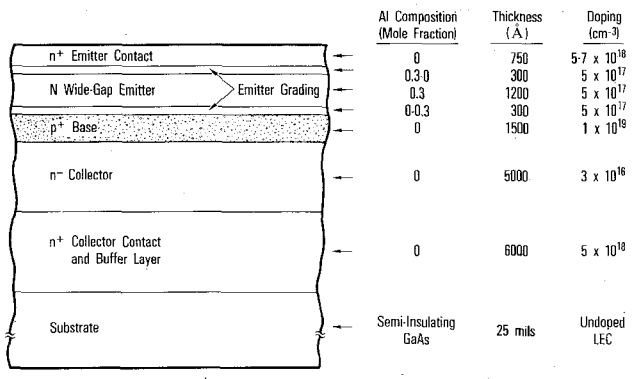


Fig. 7. Nominal GaAs/AlGaAs emitter-up n-p-n HBT growth structure fabricated with both MBE and MOCVD growth techniques for the log amp investigation.

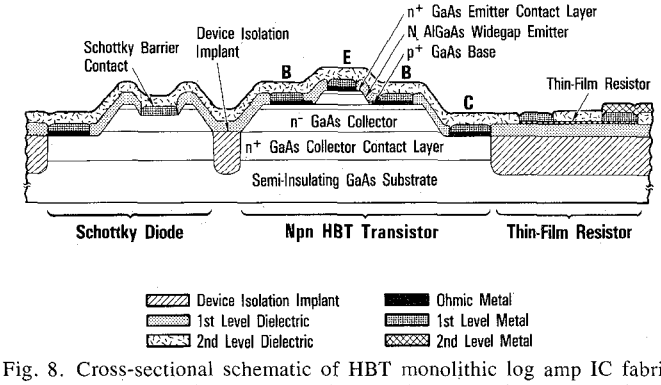
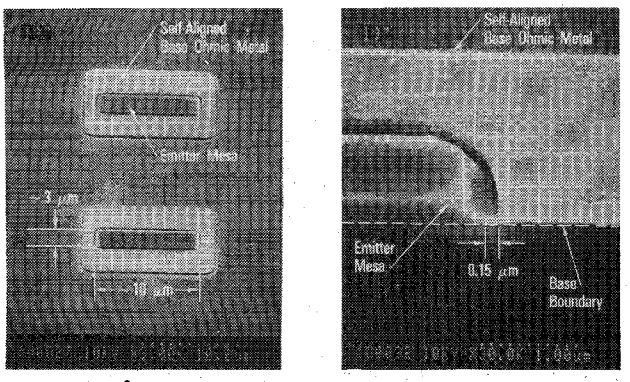


Fig. 8. Cross-sectional schematic of HBT monolithic log amp IC fabrication structure with self-aligned base ohmic metal n-p-n transistor, Schottky diode, and thin-film (nichrome) resistor.

focuses on a simplified growth structure for fabrication ease. The base layer is relatively thick and no material enhancements such as built-in drift fields or velocity overshoot structures were implemented.

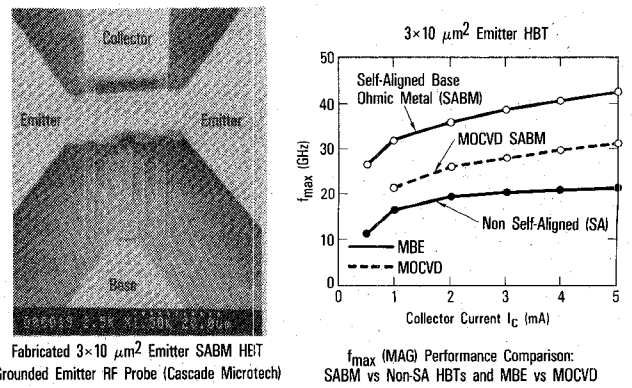
The self-aligned mesa HBT IC fabrication structure (12 mask levels), shown schematically in Fig. 8, integrates key device components including transistors, Schottky diodes, laser trimmable thin-film resistors (nichrome or cermet), and metal–insulator–metal (MIM) capacitors. For the HBT, the self-aligned base metal essentially eliminates the parasitic external base resistance, by minimizing the ohmic metal to emitter spacing, to effectively double f_{max}. A double photoresist liftoff technique is used to selectively pattern the HBT base ohmic metal to within ≈ 0.15 μm of the emitter edge, as shown by the fabricated structures in Fig. 9. The active device layers are accessed by a combination of selective and nonselective wet chemical etches. Ohmic contacts are formed by AuBe/Pd/Au and AuGe/Ni/Ti/Au for p-type and n-type ohmic contacts, respectively. A multiple boron damage implant is used for device isolation. Plasma-enhanced CVD silicon nitride is used to passivate the GaAs surface and serves as a dielectric insulator for MIM capacitors and double-level metal interconnection (TiPtAu and TiAu). TiPtAu used as the first interconnect metal also serves as the Schottky barrier metal.

The standard HBT device uses a 3 μm $\times$ 10 μm emitter–base junction. For such devices, this fabrication pro-



3×10 μm^2 Emitter HBTs (Differential Transistor Pair) Cleaved Cross-Section

Fig. 9. Scanning electron micrographs of 3 μm × 10 μm self-aligned base ohmic metal HBT transistors after ohmic metal liftoff showing a differential HBT pair and a cleaved cross-sectional structure.



Fabricated 3×10 μm^2 Emitter SABM HBT Grounded Emitter RF Probe (Cascade Microtech)

f_{max} (MAG) Performance Comparison: SABM vs Non-SA HBTs and MBE vs MOCVD

Fig. 11. Comparison of f_{max} for MBE and MOCVD 3 μm × 10 μm emitter HBT's based on the on-wafer RF probe transistor structure shown; the f_{max} was extrapolated from maximum available gain (MAG) obtained from on-wafer scattering parameter measurements to 26 GHz.

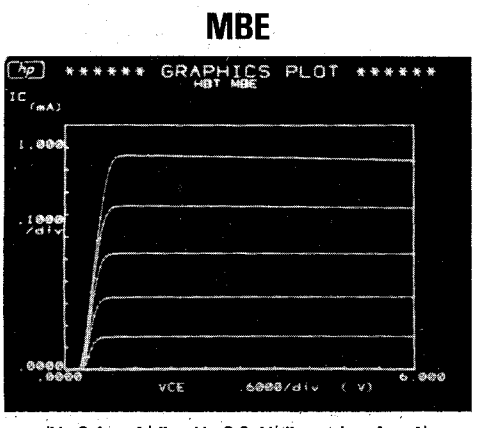
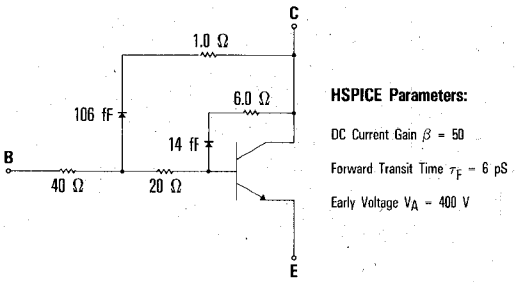


Fig. 10. Collector current (I_C) versus collector-emitter voltage (V_{CE}) characteristics of typical MBE and MOCVD 3 μm × 10 μm emitter, self-aligned base ohmic metal HBT's using the epitaxial structure of Fig. 7.



3×10 μm^2 Emitter, Self-Aligned Base Ohmic Metal HBT

Fig. 12. HSPICE transistor model for the MBE (Fig. 7) 3 μm × 10 μm emitter self-aligned base ohmic metal HBT used to simulate log amp performance.

cess demonstrates excellent transistor dc ($I_C - V_{CE}$) and RF (f_{max}) characteristics, as shown in Figs. 10 and 11, respectively, comparing both MBE and MOCVD materials. The dc current gain $\beta \approx 30$–50 ($I_C = 1$ mA) is useful for analog applications. These devices have high f_t and f_{max} in the range of $\approx$25–30 GHz at low current levels ($I_C = 1$ mA). The lower performance of the MOCVD material compared to MBE is believed to be associated with nonoptimized epitaxial growth, including base diffusion effects and lower emitter doping. From the dc and RF characteristics an HBT HSPICE device model (MBE), as described in Fig. 12, is derived for log amp circuit simulations. Both the dc β and f_t, f_{max} can be improved for MBE and MOCVD HBT's by reducing the nominal base thickness (by a factor of 2) from the relaxed 1500 Å currently used. The 3 μm emitter MBE SABM HBT's have also demonstrated 20 GHz amplifier performance, including gain $\approx$6 dB, noise figure $\approx$6 dB, and third-order intercept point $IP3$ $\approx$20 dBm for a single 3 μm × 20 μm emitter device [9]. However for the log IF amps investigated here, both MBE performance and MOCVD HBT performance exceed the circuit requirements, which result in the log amps' insensitivity to the material type, as will be seen later.

The fabricated true and successive-detection log IF amplifiers using the SABM HBT IC process are shown in Figs. 13 and 14, respectively. The true log IF amp consists of 45 HBT's and occupies a die size of 0.7 mm × 1.25 mm, while the successive-detection log IF amplifier consists of 70 HBT's and occupies a die size of 0.7 mm × 1.45 mm. On the best MBE wafer (2 in) high-speed functional yield was greater than 95 percent (33 sites tested) for both circuit types.

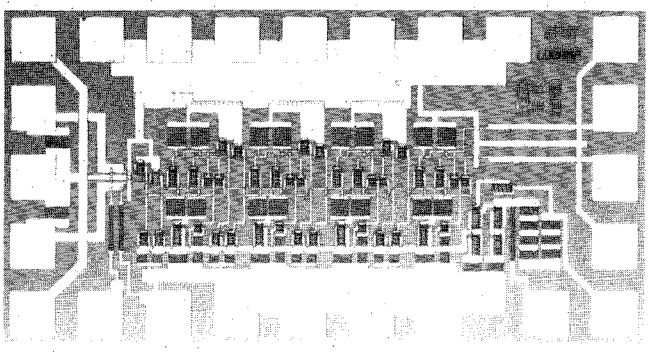


Fig. 13. Photomicrograph of a fabricated HBT monolithic four-stage true log IF amplifier (45 transistors; chip size: 0.7 mm × 1.25 mm).

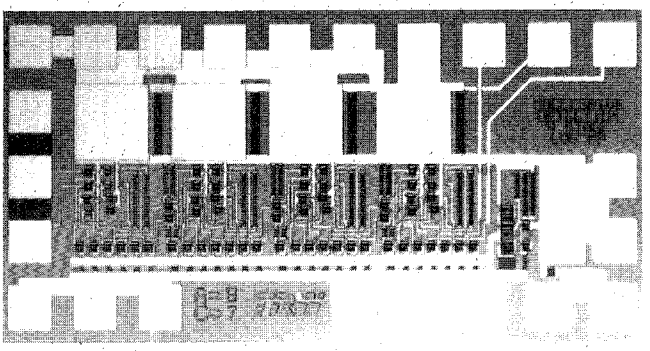


Fig. 14. Photomicrograph of a fabricated HBT monolithic four-stage successive-detection log IF amplifier (70 transistors; chip size: 0.7 mm × 1.45 mm).

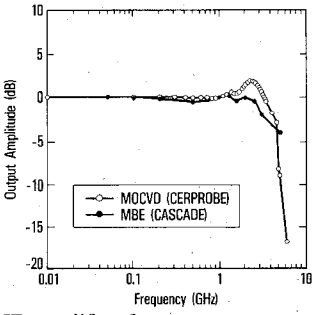
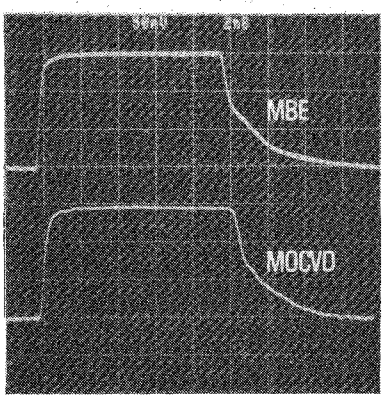


Fig. 15. True log IF amplifier frequency response measured on-wafer comparing MBE and MOCVD materials. The MOCVD log amp measurement used 50 Ω ceramic-blade probes (Cerprobe) while the MBE log amp used RF probes (Cascade Microtech). The peaking in the MOCVD log amp frequency response is due to the probe inductance.



(V: 50 mV/div; H: 2 nS/div)

Fig. 16. True log IF amplifier pulse response for MBE and MOCVD materials. The two responses are essentially identical governed by the circuit *RC* time constants; both the MBE and the MOCVD HBT frequency performance exceed the circuit requirements.

IV. HBT Log IF Amplifier Performance

Most of the log amp performance results are based on MBE fabrication; however, some MOCVD work is included for comparison. MBE was used for both true and successive-detection log amps while MOVCD was investigated only for the true log amp. The log IF circuits are essentially transparent to the material types since both MBE and MOCVD HBT performances exceed the requirements of the log amps. All log IF amplifier testing was performed on-wafer using either 50 Ω ceramic blade (Cerprobe) or RF (Cascade Microtech) probes. Key performance parameters evaluated include the frequency and pulse response, log transfer function characteristics, and log conformity (error) over the full dynamic range. The noise or tangential signal sensitivity (*TSS*) associated with the actual log bandwidth was evaluated only for the true log amp. Both the true and successive-detection log IF amplifiers use a single supply voltage of −8 V dissipating 1.06 W (133 mA) and 0.8 W (100 mA), respectively.

A. True Log IF Amplifier

The frequency response was characterized by using a synthesized signal generator for the source and a power meter to measure the output. The log amp has an input impedance of 50 Ω and an output impedance of 100 Ω. Since the power meter has a 50 Ω input impedance and is single ended, the absolute gain of the log amp is reduced by −15.6 dB. Fig. 15 shows the output response versus frequency over ≈3 GHz bandwidth for both MBE and MOCVD log amps using RF and 50 Ω ceramic blade probes, respectively. Both log amps show very similar response except for the peaking in the frequency response, which is due to probe blade inductance associated with the 50 Ω ceramic blade probe card.

The pulse response for the MBE and MOCVD log amps shown in Fig. 16 is essentially identical, governed by the circuit *RC* time constants. The pulse response of a conventional logarithmic amplifier is specified by the rise, fall, settling, and recovery times of the detected video output. These response times are limited by the video bandwidth. A typical logarithmic amplifier has a video bandwidth which is limited by the log amp circuit bandwidth and noise requirements. The video bandwidth limits the log amp rise and fall times. If the input rise and fall times are long, then the corresponding output rise and fall times will be even longer. The fall time will require several time constants to fall within 1 dB of the corresponding minimum input signal. The four-stage true log IF amp was tested as a log video amplifier with a 3 GHz bandwidth. A pulse with 0.4 ns rise and fall times was used as the input, yielding an output with 0.4 ns rise and 3.2 ns fall times, as shown in Fig. 16. This demonstrates the capability for very narrow pulse operation.

The logarithmic transfer function and log conformity

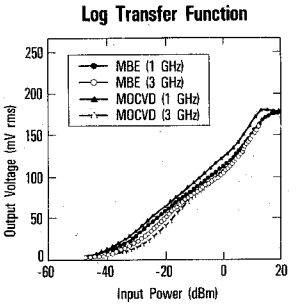


Fig. 17. True log IF amplifier transfer function characteristics comparing MBE and MOCVD for 1 and 3 GHz IF frequencies.

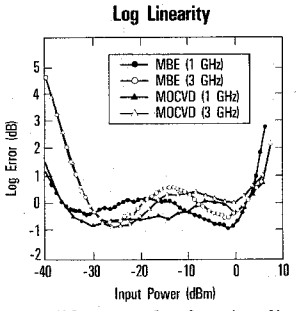


Fig. 18. True log IF amplifier transfer function linearity characteristics comparing MBE and MOCVD for 1 and 3 GHz IF frequencies.

(linearity or error) are shown in Figs. 17 and 18, respectively, for 1 and 3 GHz, again comparing MBE and MOCVD; the results are comparable for the two materials. The log transfer function is derived from the input power versus output voltage transfer curves, and from these curves a linear regression of input power versus output voltage is determined and subtracted from the actual measured transfer curve. This difference is input referred and is a measure of the logarithmic conformity. At 1 GHz the log amps have 44 dB dynamic range, maintaining $< \pm 0.85$ dB log error error, while at 3 GHz the log amps have ≈ 40 dB dynamic range with $< \pm 1$ dB log error. The dynamic range and log error designed were 48 dB and ± 1 dB, respectively. The actual dynamic range was reduced since the entire log amp is dc coupled. Any dc offset in the differential transistor pairs will be amplified by the log amp, reducing the total dynamic range. The log error is better than predicted since the log amp was designed assuming linear-limiting amplifiers. Differential pairs without emitter degeneration will have a nonlinear (pseudo-logarithmic) transfer function which will reduce the log error.

The noise or *TSS* is a measure of the noise performance of a log amp. The *TSS* is measured by reducing the input power level to a point where the signal amplitude is even (or tangential) with the noise amplitude on an oscilloscope. This input power is the *TSS* which also determines the minimum detectable signal of the log amp. The low end of the dynamic range is limited by the *TSS* or the log error, whichever is higher. The log amp *TSS* of -60 dBm shown in Fig. 19 (using a 1 GHz input signal) is limited by the available test set. By reducing the video bandwidth, the log amp *TSS* is improved.

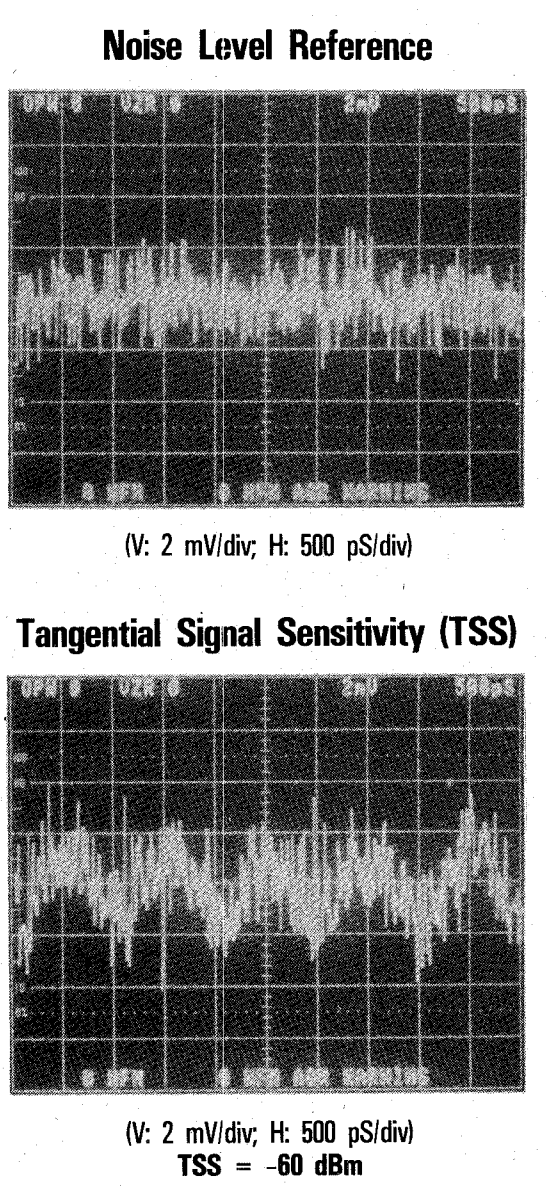


Fig. 19. True log IF amplifier (MBE) noise characteristics showing the reference noise level and tangential signal sensitivity (*TSS*) of -60 dBm using a 1 GHz IF input. The measured *TSS* of the log amp is test set limited.

B. Successive-Detection Log IF Amplifier

The frequency response of the MBE successive-detection log amp was characterized by using a synthesized signal generator for the source and a real-time oscilloscope to measure the video output. The log amp has an input impedance of 50 Ω and a video output impedance of 175 Ω, tested into a 50 Ω load. Unloaded, this log IF has a video bandwidth of 200 MHz. Loading changes the video frequency, necessitating an external video filter. Conventional log amplifier frequency response is specified by measuring the output voltage reduction for a constant input power as a function of frequency and dividing this by the log slope. This will be the log amplifier frequency response which is shown in Fig. 20. The successive-detection log amp's input-referred, -3 dB frequency is 550 MHz. The frequency response is limited by the use

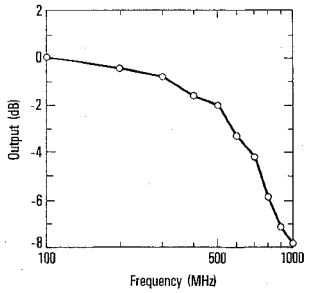
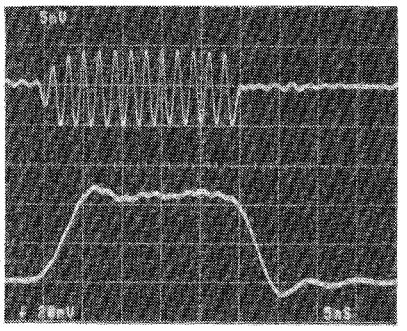


Fig. 20. Successive-detection log IF amplifier (MBE) frequency response measured on-wafer with 50 Ω ceramic blade probes (Cerprobe).



(V: 5 mV/div; H: 5 nS/div)
Top: Input Pulse (500 MHz IF)
Bottom: Detected Video Output

Fig. 21. Successive-detection log IF amplifier (MBE) pulse response showing the video input pulse burst and the detected video output.

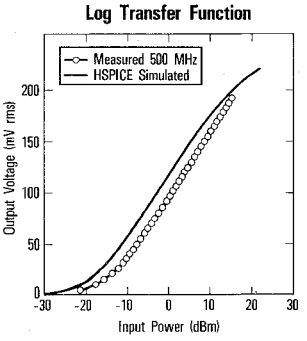


Fig. 22. Successive-detection log IF amplifier (MBE) transfer function characteristics comparing measured and HSPICE simulated results.

of large load resistors, chosen to linearize the individual limiting amplifiers and increase their output dynamic range to ensure proper operation of the full-wave detectors. This reduces the −3 dB frequency of each amplifier to 2.5 GHz and thus the cascaded frequency response to 550 MHz.

The log amp pulse response was measured by inputting an RF pulse burst and measuring the detected pulse output. The pulse response of the log amp is shown in Fig. 21. The RF frequency is 500 MHz and the pulse burst width is 25 ns. The log amp rise time (10–90 percent) shown is limited by the input pulse burst rise time ≈5 ns (limited by the test set hybrid switch). An external 160 MHz filter was used to filter the video output. The overshoot is caused by probe blade inductance. The fall time (90–10 percent) is less than 5.2 ns.

The logarithmic transfer function and log error were

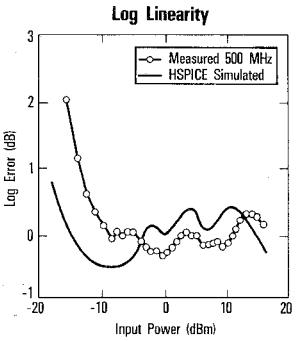


Fig. 23. Successive-detection log IF amplifier (MBE) transfer function linearity characteristics comparing measured and HSPICE simulated results.

characterized by inputting a 500 MHz signal and monitoring the dc video output. The corresponding transfer function is shown in Fig. 22. Fig. 23 shows the log linearity, which is the input-referred error of the measured transfer function from a best-fit straight line. The transfer response, over which the log amp has usable log linearity, is weighted toward the higher input power levels. This is due to a conservative full-wave detector design which reduces the detector sensitivity. As shown in these figures, SPICE simulations of the log amp circuit correlate well with the measured results.

V. Summary and Conclusions

The first GaAs/AlGaAs HBT logarithmic amplifiers have been demonstrated, advancing the state-of-the-art performance. Monolithic four-stage true and successive-detection logarithmic IF amplifiers based on Si bipolar designs were used to achieve high performance with low power consumption and small size. The log IF amplifiers were fabricated with an advanced HBT fabrication process based on both MBE and MOCVD epitaxy and self-aligned base ohmic metal transistors designed for RF analog IC applications. The HBT f_t and f_{max} in the range of 20–40 GHz permitted circuit design limited IF performance. The true log IF amplifiers have yielded the highest IF input frequency capability, ≈3 GHz, the lowest power consumption, ≈1 W, for a monolithic dynamic range of ≈40 dB and a log error $< \pm 1$ dB, an operational bandwidth of ≈dc to 3 GHz, very narrow pulse resolution, and a tangential signal sensitivity of −60 dBm (test set limited). The successive-detection log IF amplifier demonstrated a combination of high bandwidth, ≈550 MHz, with $< \pm 0.34$ dB log error over 27 dB dynamic range. These results verify the capability of the HBT technology to advance the monolithic log amp performance beyond those based on current Si bipolar and GaAs MESFET techniques. Refined fabrication and circuit designs are expected to yield HBT monolithic log IF amplifiers with even greater improvements in combined performance, power consumption, size, and cost.

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Iiyama, R. Dobbins, E. Matthews, F. Ramirez, R. Wang, S. Wolverton, J. DiMond, K. Stolt, and V. Mulvey of the Advanced Microelectronics Laboratory.

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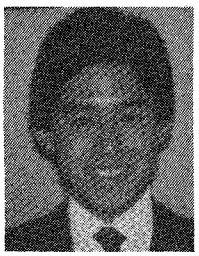

A. K. Oki (M'85) was born in Honolulu, HI, on March 20, 1961. He received the B.S. degree in electrical engineering from the University of Hawaii in 1983 and the M.S. degree in electrical engineering from the University of California, Berkeley, in 1985. At the University of Hawaii he served as a teaching assistant on semiconductor fabrication technology.

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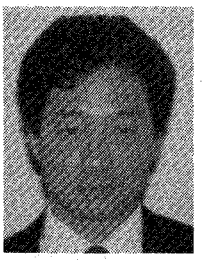

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Dr. Kim is a member of the American Physical Society.

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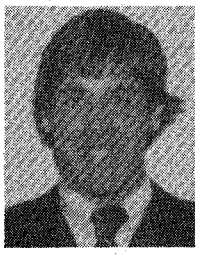

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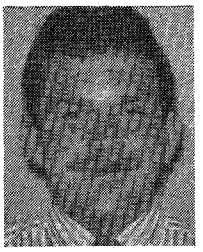

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After his degree he joined TRW to work on GaAs MESFET and HBT technologies. He is currently a Member of the Technical Staff in the GaAs Integrated Circuits Department in TRW's Electronics and Technology Division, Redondo Beach, CA. He contributed to the development of TRW's baseline non-self-aligned HBT IC process. He is currently involved with the development of advanced self-aligned HBT technologies with focus on process development for A/D, digital, analog, and microwave/millimeter-wave applications. Key HBT circuit developments to which he has contributed include flash A/D converters, sample-and-hold circuits, and RF analog IC's such as log amps, multipliers, and switches.